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Page(s): 352 -361[\[Abstract\]](#) [\[PDF Full-Text \(960 KB\)\]](#) **IEEE JNL****47 Access graphs: a model for investigating memory consistency***Linder, D.H.; Harden, J.C.;*

Parallel and Distributed Systems, IEEE Transactions on , Volume: 5 Issue: 1 , J 1994

Page(s): 39 -52

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1. Document ID: US 6157981 A

L3: Entry 1 of 12 File: USPT Dec 5, 2000

US-PAT-NO: 6157981  
DOCUMENT-IDENTIFIER: US 6157981 A

TITLE: Real time invariant behavior cache

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KMC
Draw Desc	Image										

2. Document ID: US 5983336 A

L3: Entry 2 of 12 File: USPT Nov 9, 1999

US-PAT-NO: 5983336  
DOCUMENT-IDENTIFIER: US 5983336 A

TITLE: Method and apparatus for packing and unpacking wide instruction word using pointers and masks to shift word syllables to designated execution units groups

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KMC
Draw Desc	Image										

3. Document ID: US 5923871 A

L3: Entry 3 of 12 File: USPT Jul 13, 1999

US-PAT-NO: 5923871  
DOCUMENT-IDENTIFIER: US 5923871 A

TITLE: Multifunctional execution unit having independently operable adder and multiplier

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KMC
Draw Desc	Image										

4. Document ID: US 5889985 A

L3: Entry 4 of 12 File: USPT Mar 30, 1999

US-PAT-NO: 5889985  
DOCUMENT-IDENTIFIER: US 5889985 A



TITLE: Array prefetch apparatus and method

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC
Draw Desc	Image										

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☐ 5. Document ID: US 5408626 A

L3: Entry 5 of 12

File: USPT

Apr 18, 1995

US-PAT-NO: 5408626

DOCUMENT-IDENTIFIER: US 5408626 A

TITLE: One clock address pipelining in segmentation unit

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	KWIC
Draw Desc	Image									

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☐ 6. Document ID: US 5226129 A

L3: Entry 6 of 12

File: USPT

Jul 6, 1993

US-PAT-NO: 5226129

DOCUMENT-IDENTIFIER: US 5226129 A

TITLE: Program counter and indirect address calculation system which concurrently performs updating of a program counter and generation of an effective address

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	KWIC
Draw Desc	Image									

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☐ 7. Document ID: US 5136696 A

L3: Entry 7 of 12

File: USPT

Aug 4, 1992

US-PAT-NO: 5136696

DOCUMENT-IDENTIFIER: US 5136696 A

TITLE: High-performance pipelined central processor for predicting the occurrence of executing single-cycle instructions and multicycle instructions

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	KWIC
Draw Desc	Image									

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☐ 8. Document ID: US 4342080 A

L3: Entry 8 of 12

File: USPT

Jul 27, 1982

US-PAT-NO: 4342080

DOCUMENT-IDENTIFIER: US 4342080 A

TITLE: Computer with microcode generator system

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
Draw Desc	Image								

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☐ 9. Document ID: US 4302809 A

L3: Entry 9 of 12

File: USPT

Nov 24, 1981

US-PAT-NO: 4302809

DOCUMENT-IDENTIFIER: US 4302809 A

TITLE: External data store memory device

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
Draw Desc	Image								

KMIC

☐ 10. Document ID: US 4218757 A

L3: Entry 10 of 12

File: USPT

Aug 19, 1980

US-PAT-NO: 4218757

DOCUMENT-IDENTIFIER: US 4218757 A

TITLE: Device for automatic modification of ROM contents by a system selected variable

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
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KMIC

☐ 11. Document ID: US 4138738 A

L3: Entry 11 of 12

File: USPT

Feb 6, 1979

US-PAT-NO: 4138738

DOCUMENT-IDENTIFIER: US 4138738 A

TITLE: Self-contained relocatable memory subsystem

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
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☐ 12. Document ID: US 3976978 A

L3: Entry 12 of 12

File: USPT

Aug 24, 1976

US-PAT-NO: 3976978

DOCUMENT-IDENTIFIER: US 3976978 A

TITLE: Method of generating addresses to a paged memory

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
Draw	Desc	Image							

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Term	Documents
EFFECTIVE.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	1396775
EFFECTIVES.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	53
ADDRESS\$3	0
ADDRESS.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	455570
ADDRESSA.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	15
ADDRESSAB.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	4
ADDRESSABE.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	7
ADDRESSABL.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	1
ADDRESSACK.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	2
ADDRESSAGE.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	1
ADDRESSAL.DWPI,TDBD,EPAB,JPAB,USPT,PGPB.	2
(EFFECTIVE NEAR3 ADDRESS\$3 NEAR5 INSTRUCTION\$ NEAR8 (RELATIVE OR RELATIONSHIP\$) NEAR5 ADDRESS\$3).USPT,PGPB,JPAB,EPAB,DWPI,TDBD.	12

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L3: Entry 1 of 2

File: USPT

Mar 19, 2002

US-PAT-NO: 6360314

DOCUMENT-IDENTIFIER: US 6360314 B1

TITLE: Data cache having store queue bypass for out-of-order instruction execution  
and method for same

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KMC
Draw Desc	Image										

☐ 2. Document ID: US 5751946 A

L3: Entry 2 of 2

File: USPT

May 12, 1998

US-PAT-NO: 5751946

DOCUMENT-IDENTIFIER: US 5751946 A

TITLE: Method and system for detecting bypass error conditions in a load/store unit  
of a superscalar processor

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	KMC
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Term	Documents
LOAD	1283606
LOADS	288248
STORE	495800
STORES	511984
ADDRESS	530668
ADDRESSES	219785
COMPAR\$5	0
COMPAR	4018
COMPARA	4497
COMPARAATOR	5
COMPARABALE	5
(LOAD NEAR5 STORE NEAR5 ADDRESS NEAR4 COMPAR\$5 NEAR10 BYPASS\$3).USPT,PGPB,JPAB,EPAB,DWPI,TDBD.	2

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L27: Entry 1 of 27

File: USPT

Dec 24, 2002

US-PAT-NO: 6499098

DOCUMENT-IDENTIFIER: US 6499098 B1

TITLE: Processor with instruction qualifiers to control MMU operation

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KMC
Draw Desc	Image										

☐ 2. Document ID: US 6430679 B1

L27: Entry 2 of 27

File: USPT

Aug 6, 2002

US-PAT-NO: 6430679

DOCUMENT-IDENTIFIER: US 6430679 B1

TITLE: Pre-arbitrated bypasssing in a speculative execution microprocessor

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KMC
Draw Desc	Image										

☐ 3. Document ID: US 6314504 B1

L27: Entry 3 of 27

File: USPT

Nov 6, 2001

US-PAT-NO: 6314504

DOCUMENT-IDENTIFIER: US 6314504 B1

**\*\* See image for Certificate of Correction \*\***

TITLE: Multi-mode memory addressing using variable-length

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KMC
Draw Desc	Image										

☐ 4. Document ID: US 6282633 B1

L27: Entry 4 of 27

File: USPT

Aug 28, 2001

US-PAT-NO: 6282633

DOCUMENT-IDENTIFIER: US 6282633 B1

TITLE: High data density RISC processor

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC
Draw Desc	Image										

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☐ 5. Document ID: US 6272619 B1

L27: Entry 5 of 27

File: USPT

Aug 7, 2001

US-PAT-NO: 6272619

DOCUMENT-IDENTIFIER: US 6272619 B1

TITLE: High-performance, superscalar-based computer system with out-of-order instruction execution

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC
Draw Desc	Image										

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☐ 6. Document ID: US 6256720 B1

L27: Entry 6 of 27

File: USPT

Jul 3, 2001

US-PAT-NO: 6256720

DOCUMENT-IDENTIFIER: US 6256720 B1

TITLE: High performance, superscalar-based computer system with out-of-order instruction execution

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC
Draw Desc	Image										

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☐ 7. Document ID: US 6212629 B1

L27: Entry 7 of 27

File: USPT

Apr 3, 2001

US-PAT-NO: 6212629

DOCUMENT-IDENTIFIER: US 6212629 B1

TITLE: Method and apparatus for executing string instructions

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC
Draw Desc	Image										

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☐ 8. Document ID: US 6189088 B1

L27: Entry 8 of 27

File: USPT

Feb 13, 2001

US-PAT-NO: 6189088

DOCUMENT-IDENTIFIER: US 6189088 B1

TITLE: Forwarding stored data fetched for out-of-order load/read operation to over-taken operation read-accessing same memory location

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
Draw Desc	Image								

KMIC

☐ 9. Document ID: US 6145074 A

L27: Entry 9 of 27

File: USPT

Nov 7, 2000

US-PAT-NO: 6145074

DOCUMENT-IDENTIFIER: US 6145074 A

**\*\* See image for Certificate of Correction \*\***

TITLE: Selecting register or previous instruction result bypass as source operand path based on bypass specifier field in succeeding instruction

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
Draw Desc	Image								

KMIC

☐ 10. Document ID: US 6128723 A

L27: Entry 10 of 27

File: USPT

Oct 3, 2000

US-PAT-NO: 6128723

DOCUMENT-IDENTIFIER: US 6128723 A

TITLE: High-performance, superscalar-based computer system with out-of-order instruction execution

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
Draw Desc	Image								

KMIC

☐ 11. Document ID: US 6101594 A

L27: Entry 11 of 27

File: USPT

Aug 8, 2000

US-PAT-NO: 6101594

DOCUMENT-IDENTIFIER: US 6101594 A

TITLE: High-performance, superscalar-based computer system with out-of-order instruction execution

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
Draw Desc	Image								

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☐ 12. Document ID: US 6092181 A

L27: Entry 12 of 27

File: USPT

Jul 18, 2000

US-PAT-NO: 6092181

DOCUMENT-IDENTIFIER: US 6092181 A

**\*\* See image for Certificate of Correction \*\***



TITLE: High-performance, superscalar-based computer system with out-of-order instruction execution

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	KWIC
Draw Desc	Image									

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☐ 13. Document ID: US 6092177 A

L27: Entry 13 of 27

File: USPT

Jul 18, 2000

US-PAT-NO: 6092177

DOCUMENT-IDENTIFIER: US 6092177 A

TITLE: Computer architecture capable of execution of general purpose multiple instructions

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	KWIC
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☐ 14. Document ID: US 6038654 A

L27: Entry 14 of 27

File: USPT

Mar 14, 2000

US-PAT-NO: 6038654

DOCUMENT-IDENTIFIER: US 6038654 A

**\*\* See image for Certificate of Correction \*\***

TITLE: High performance, superscalar-based computer system with out-of-order instruction execution

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	KWIC
Draw Desc	Image									

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☐ 15. Document ID: US 6016543 A

L27: Entry 15 of 27

File: USPT

Jan 18, 2000

US-PAT-NO: 6016543

DOCUMENT-IDENTIFIER: US 6016543 A

TITLE: Microprocessor for controlling the conditional execution of instructions

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	KWIC
Draw Desc	Image									

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☐ 16. Document ID: US 6016532 A

L27: Entry 16 of 27

File: USPT

Jan 18, 2000

US-PAT-NO: 6016532

DOCUMENT-IDENTIFIER: US 6016532 A

TITLE: Method for handling data cache misses using help instructions

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	KWIC
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☐ 17. Document ID: US 5968163 A

L27: Entry 17 of 27

File: USPT

Oct 19, 1999

US-PAT-NO: 5968163

DOCUMENT-IDENTIFIER: US 5968163 A

TITLE: Microcode scan unit for scanning microcode instructions using predecode data

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	KWIC
Draw Desc	Image									

☐ 18. Document ID: US 5909567 A

L27: Entry 18 of 27

File: USPT

Jun 1, 1999

US-PAT-NO: 5909567

DOCUMENT-IDENTIFIER: US 5909567 A

TITLE: Apparatus and method for native mode processing in a RISC-based CISC processor

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	KWIC
Draw Desc	Image									

☐ 19. Document ID: US 5878252 A

L27: Entry 19 of 27

File: USPT

Mar 2, 1999

US-PAT-NO: 5878252

DOCUMENT-IDENTIFIER: US 5878252 A

TITLE: Microprocessor configured to generate help instructions for performing data cache fills

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	KWIC
Draw Desc	Image									

☐ 20. Document ID: US 5852727 A

L27: Entry 20 of 27

File: USPT

Dec 22, 1998

US-PAT-NO: 5852727

DOCUMENT-IDENTIFIER: US 5852727 A

TITLE: Instruction scanning unit for locating instructions via parallel scanning of start and end byte information

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
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LOADS	288338
STORE	496028
STORES	512563
BYPASS\$3	0
BYPASS	142822
BYPASSA	1
BYPASSABL	1
BYPASSAED	1
BYPASSAGE	34
BYPASSCMD	9
(L18 AND LOAD NEAR8 STORE AND BYPASS\$3 NEAR6 ADDRESS\$3).USPT,PGPB,JPAB,EPAB,DWPI,TDBD.	27

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L27: Entry 21 of 27

File: USPT

Nov 10, 1998

US-PAT-NO: 5835968

DOCUMENT-IDENTIFIER: US 5835968 A

TITLE: Apparatus for providing memory and register operands concurrently to functional units

<a href="#">Full</a>	<a href="#">Title</a>	<a href="#">Citation</a>	<a href="#">Front</a>	<a href="#">Review</a>	<a href="#">Classification</a>	<a href="#">Date</a>	<a href="#">Reference</a>	<a href="#">Sequences</a>	<a href="#">Attachments</a>	<a href="#">KVMC</a>
<a href="#">Draw Desc</a>	<a href="#">Image</a>									

☐ 22. Document ID: US 5758195 A

L27: Entry 22 of 27

File: USPT

May 26, 1998

US-PAT-NO: 5758195

DOCUMENT-IDENTIFIER: US 5758195 A

TITLE: Register to memory data transfers with field extraction and zero/sign extension based upon size and mode data corresponding to employed address register

<a href="#">Full</a>	<a href="#">Title</a>	<a href="#">Citation</a>	<a href="#">Front</a>	<a href="#">Review</a>	<a href="#">Classification</a>	<a href="#">Date</a>	<a href="#">Reference</a>	<a href="#">Sequences</a>	<a href="#">Attachments</a>	<a href="#">KVMC</a>
<a href="#">Draw Desc</a>	<a href="#">Image</a>									

☐ 23. Document ID: US 5689720 A

L27: Entry 23 of 27

File: USPT

Nov 18, 1997

US-PAT-NO: 5689720

DOCUMENT-IDENTIFIER: US 5689720 A

TITLE: High-performance superscalar-based computer system with out-of-order instruction execution

<a href="#">Full</a>	<a href="#">Title</a>	<a href="#">Citation</a>	<a href="#">Front</a>	<a href="#">Review</a>	<a href="#">Classification</a>	<a href="#">Date</a>	<a href="#">Reference</a>	<a href="#">Sequences</a>	<a href="#">Attachments</a>	<a href="#">KVMC</a>
<a href="#">Draw Desc</a>	<a href="#">Image</a>									

☐ 24. Document ID: US 5006980 A

L27: Entry 24 of 27

File: USPT

Apr 9, 1991

US-PAT-NO: 5006980

DOCUMENT-IDENTIFIER: US 5006980 A

**\*\* See image for Certificate of Correction \*\***

TITLE: Pipelined digital CPU with deadlock resolution

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	KMC
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☐ 25. Document ID: US 4875160 A

L27: Entry 25 of 27

File: USPT

Oct 17, 1989

US-PAT-NO: 4875160

DOCUMENT-IDENTIFIER: US 4875160 A

**\*\* See image for Certificate of Correction \*\***

TITLE: Method for implementing synchronous pipeline exception recovery

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	KMC
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☐ 26. Document ID: US 4493027 A

L27: Entry 26 of 27

File: USPT

Jan 8, 1985

US-PAT-NO: 4493027

DOCUMENT-IDENTIFIER: US 4493027 A

TITLE: Method of performing a call operation in a digital data processing system having microcode call and return operations

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	KMC
Draw Desc	Image									

☐ 27. Document ID: US 4445177 A

L27: Entry 27 of 27

File: USPT

Apr 24, 1984

US-PAT-NO: 4445177

DOCUMENT-IDENTIFIER: US 4445177 A

TITLE: Digital data processing system utilizing a unique arithmetic logic unit for handling uniquely identifiable addresses for operands and instructions

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	KMC
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BYPASSABL	1
BYPASSAED	1
BYPASSAGE	34
BYPASSCMD	9
(L18 AND LOAD NEAR8 STORE AND BYPASS\$3 NEAR6 ADDRESS\$3).USPT,PGPB,JPAB,EPAB,DWPI,TDBD.	27

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